

Figure 1 - Overview Block Diagram

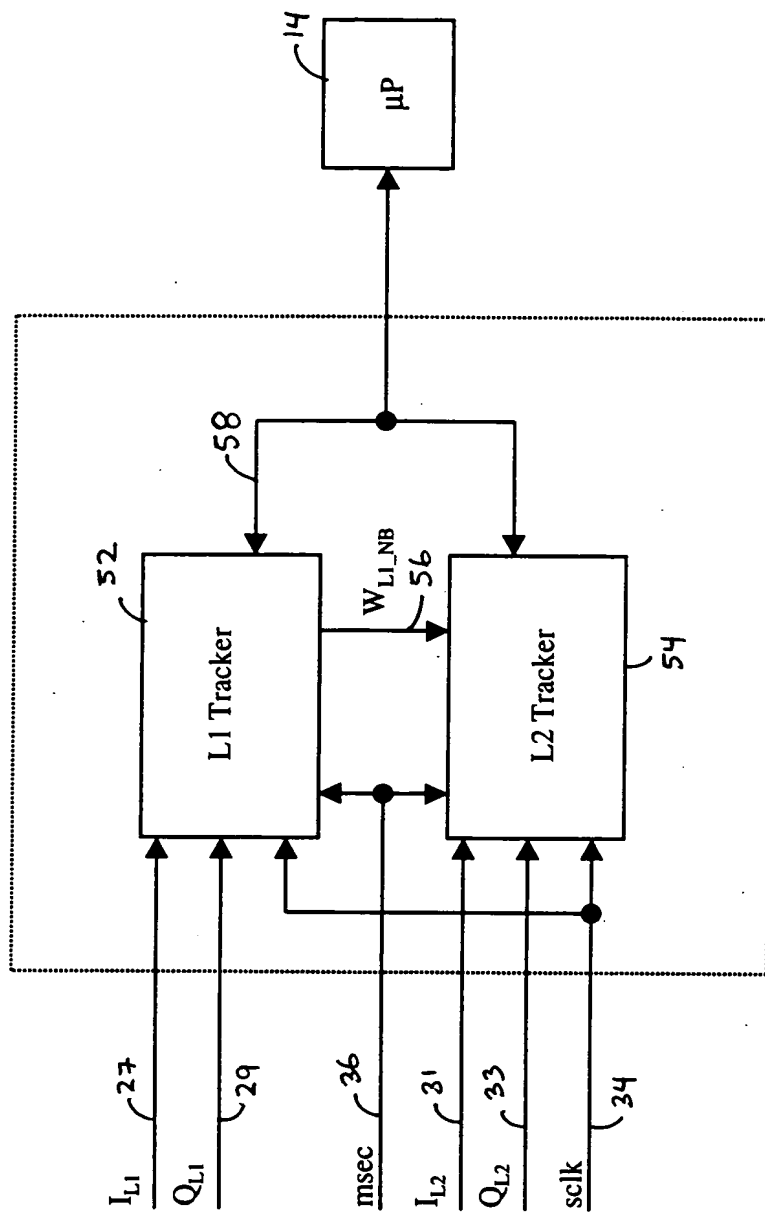
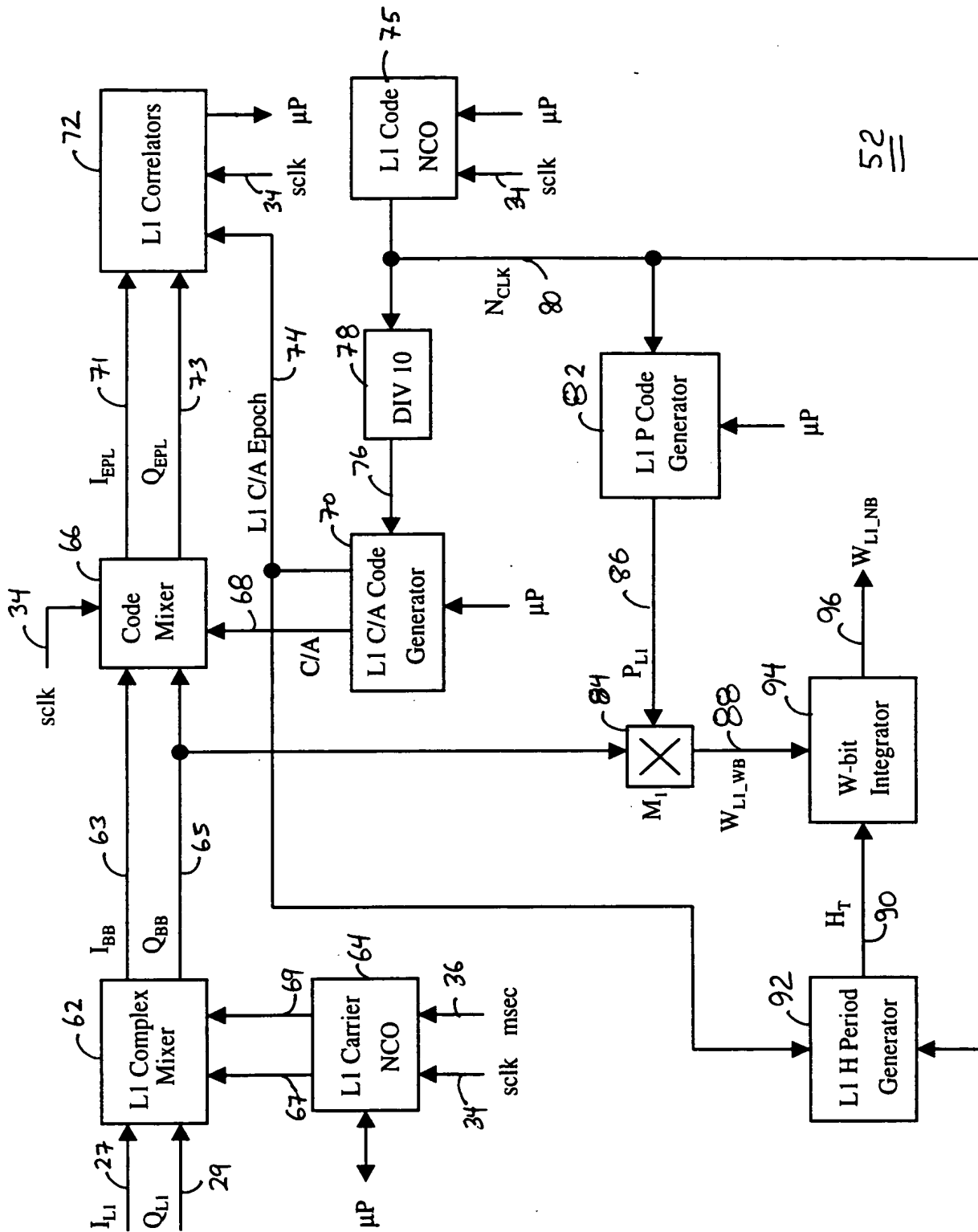


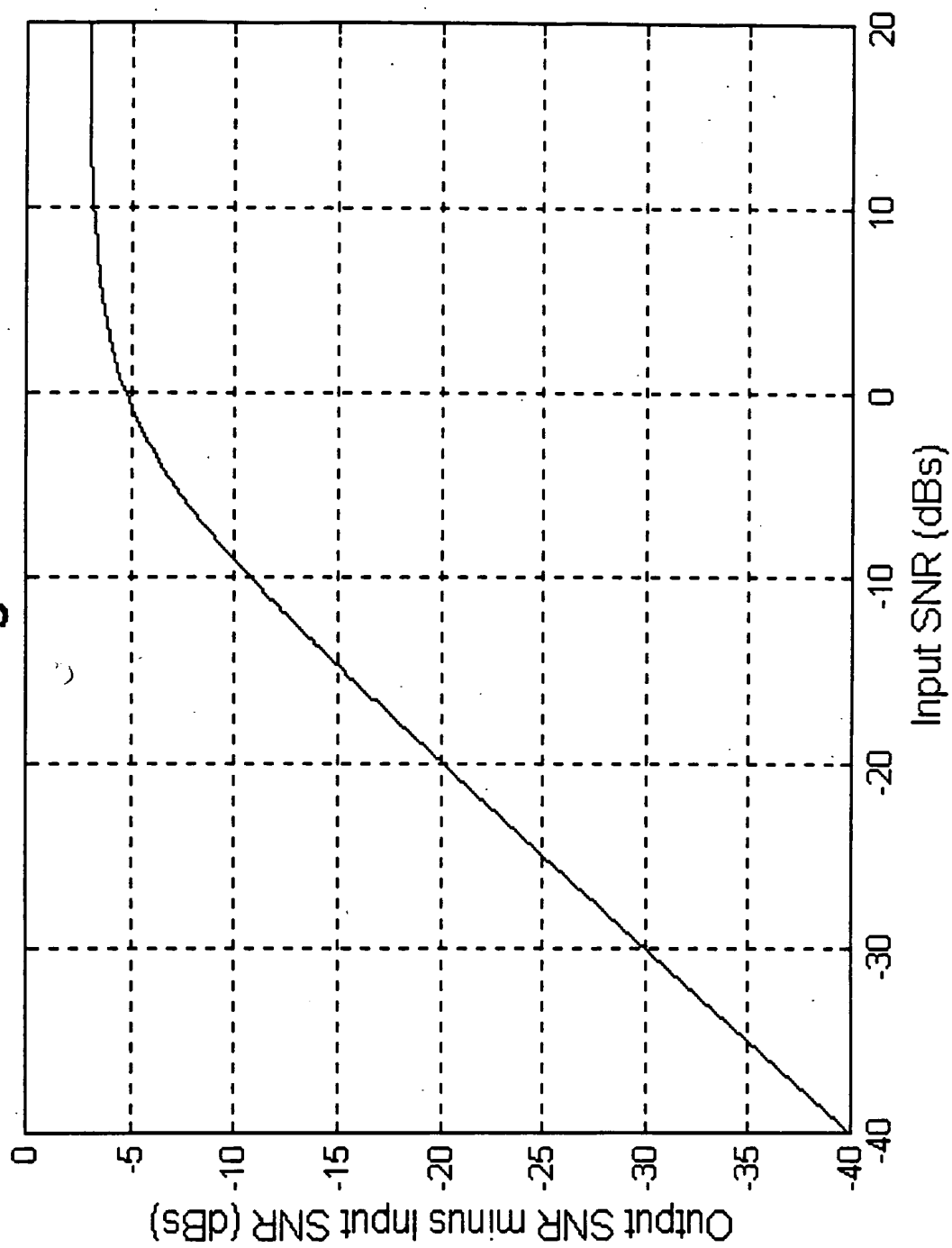
Figure 2 - L1/L2 Digital Channel Processor



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Figure 3 - L1 Tracker

Figure 4



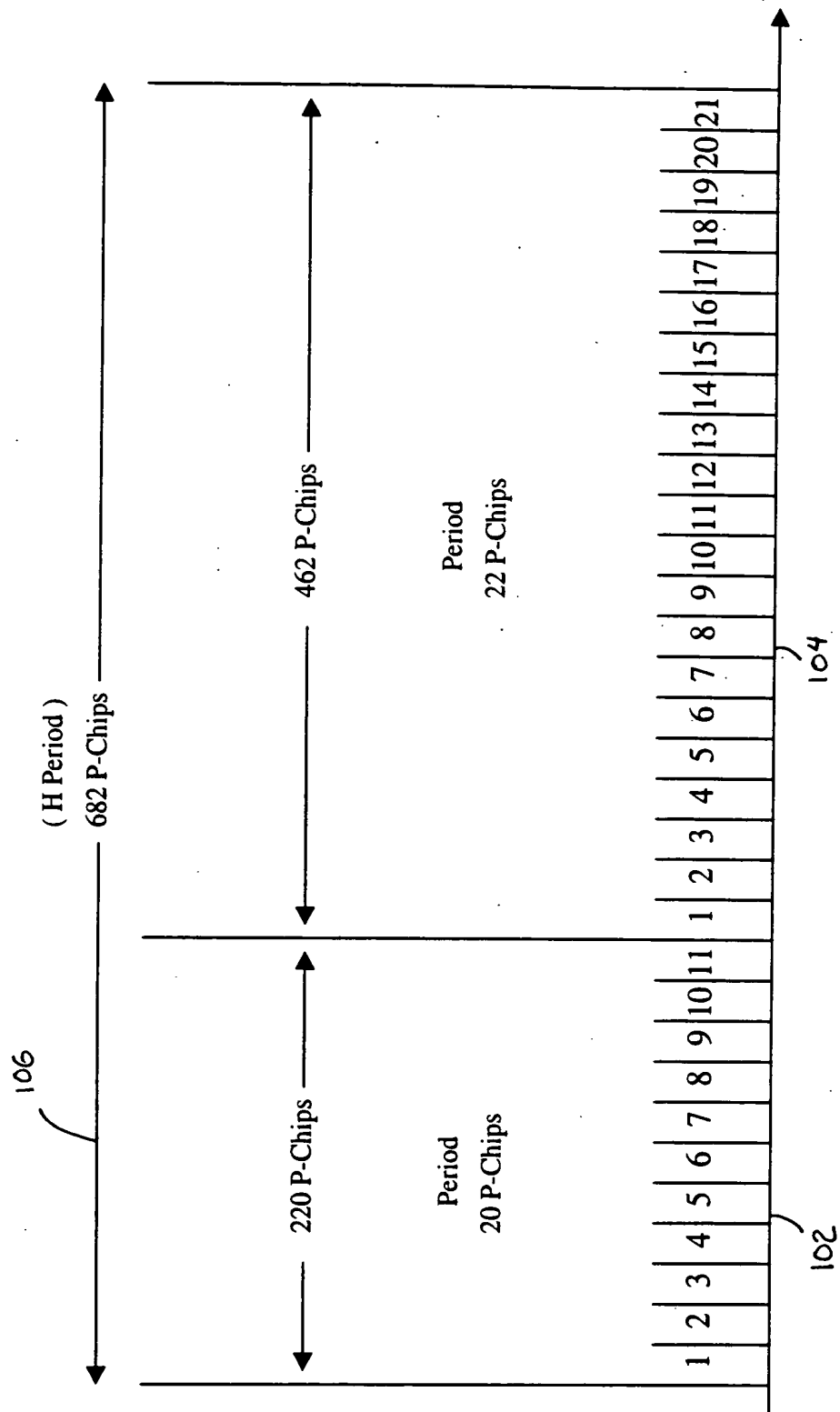
100

Figure 5a - H Period description - Part 1

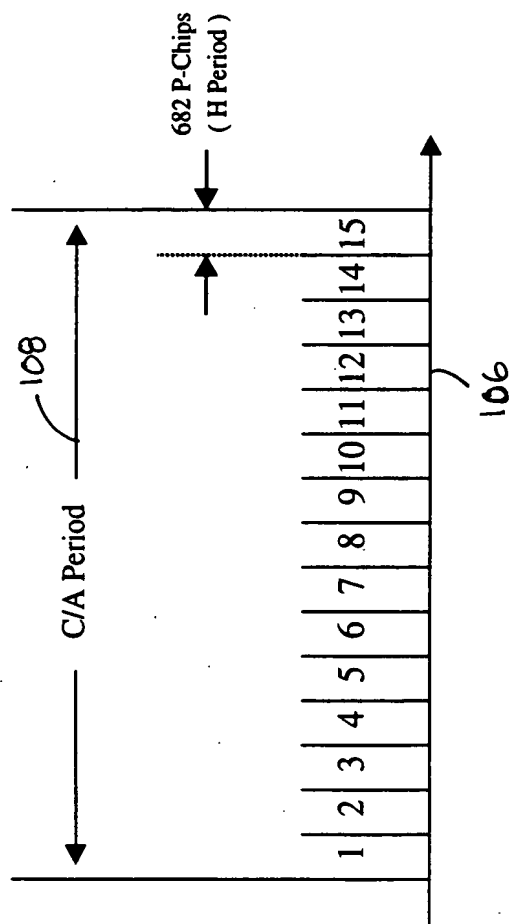
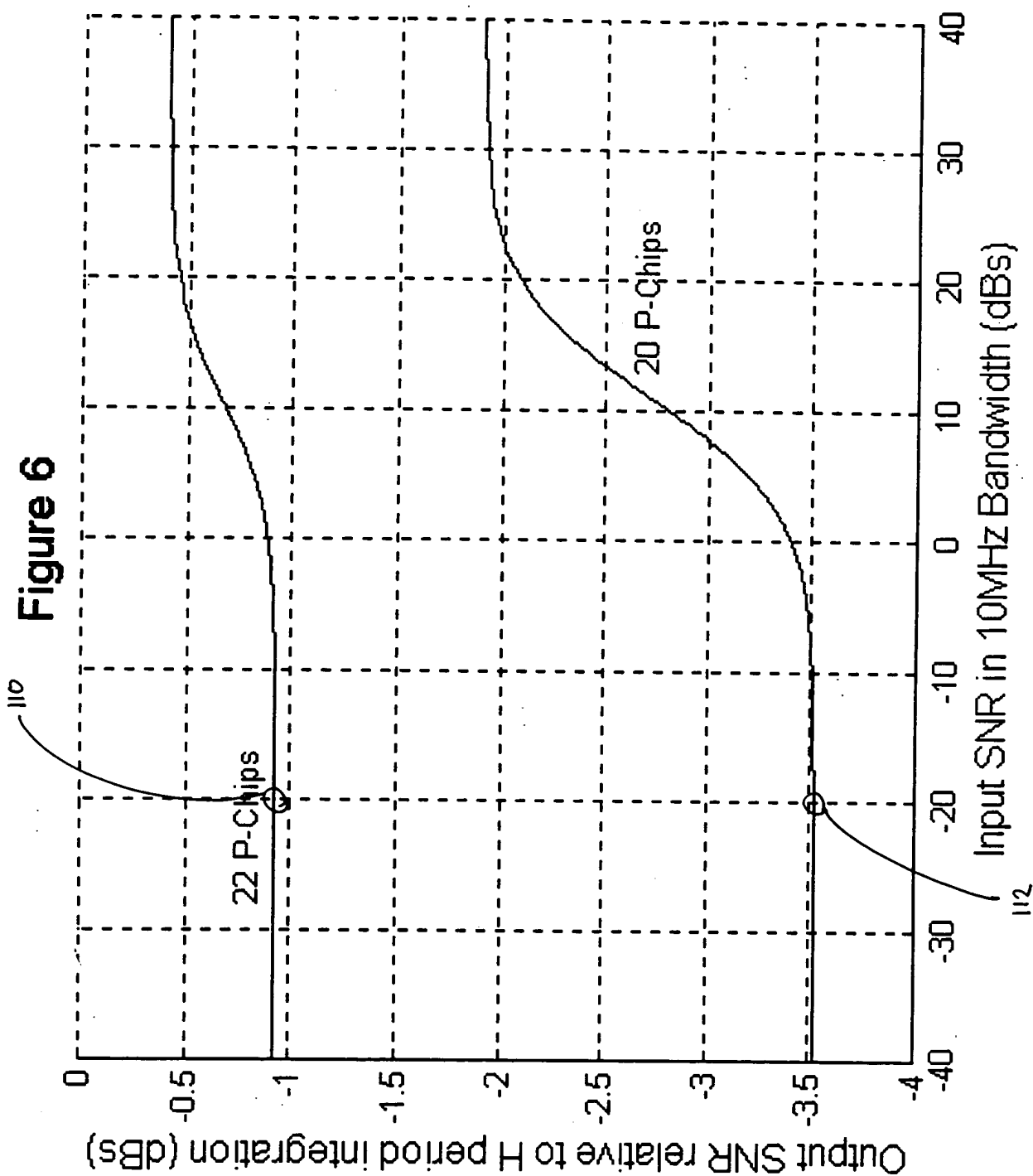


Figure 5b - H Period description - Part 2



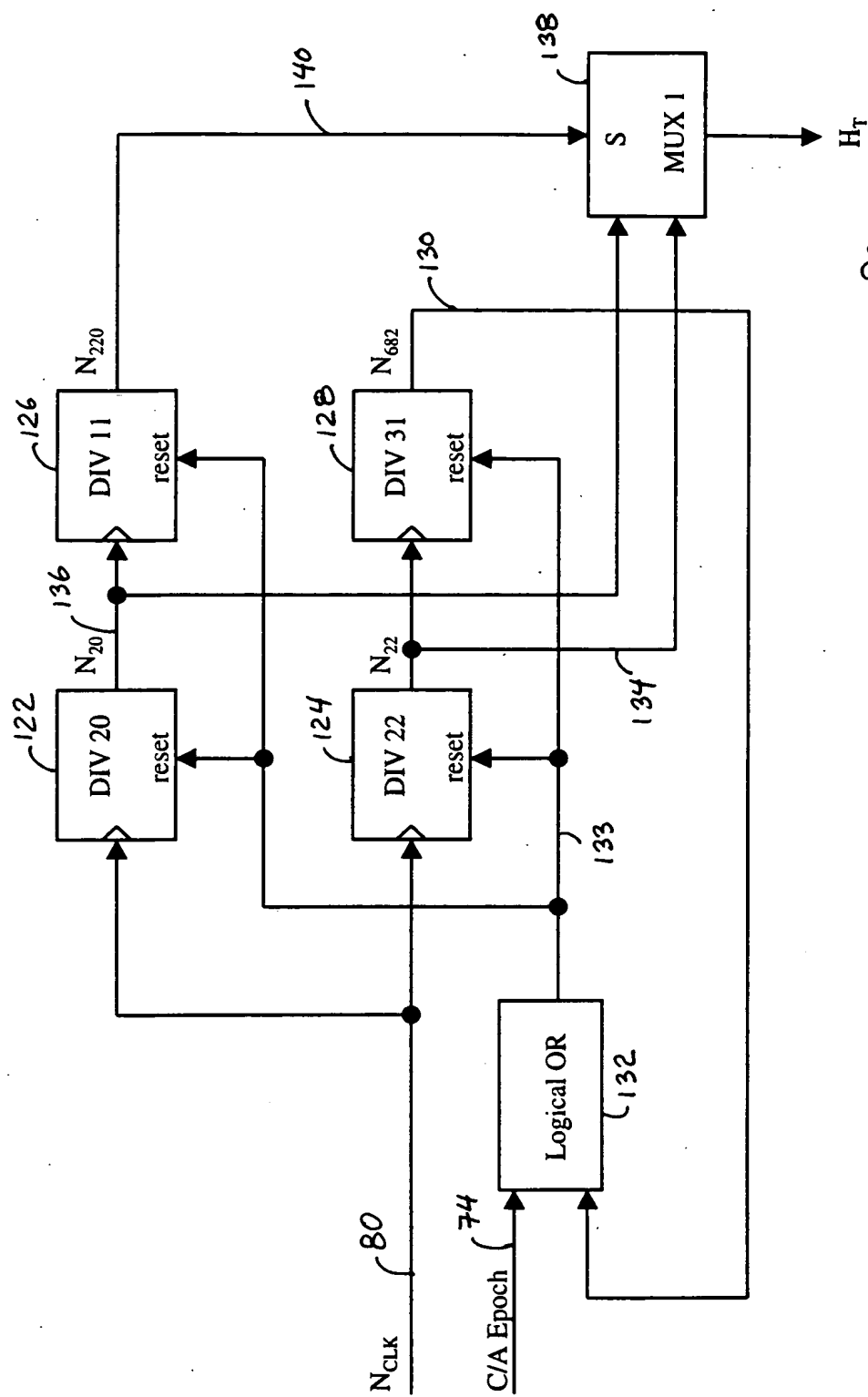


Figure 7 - H Period Generator



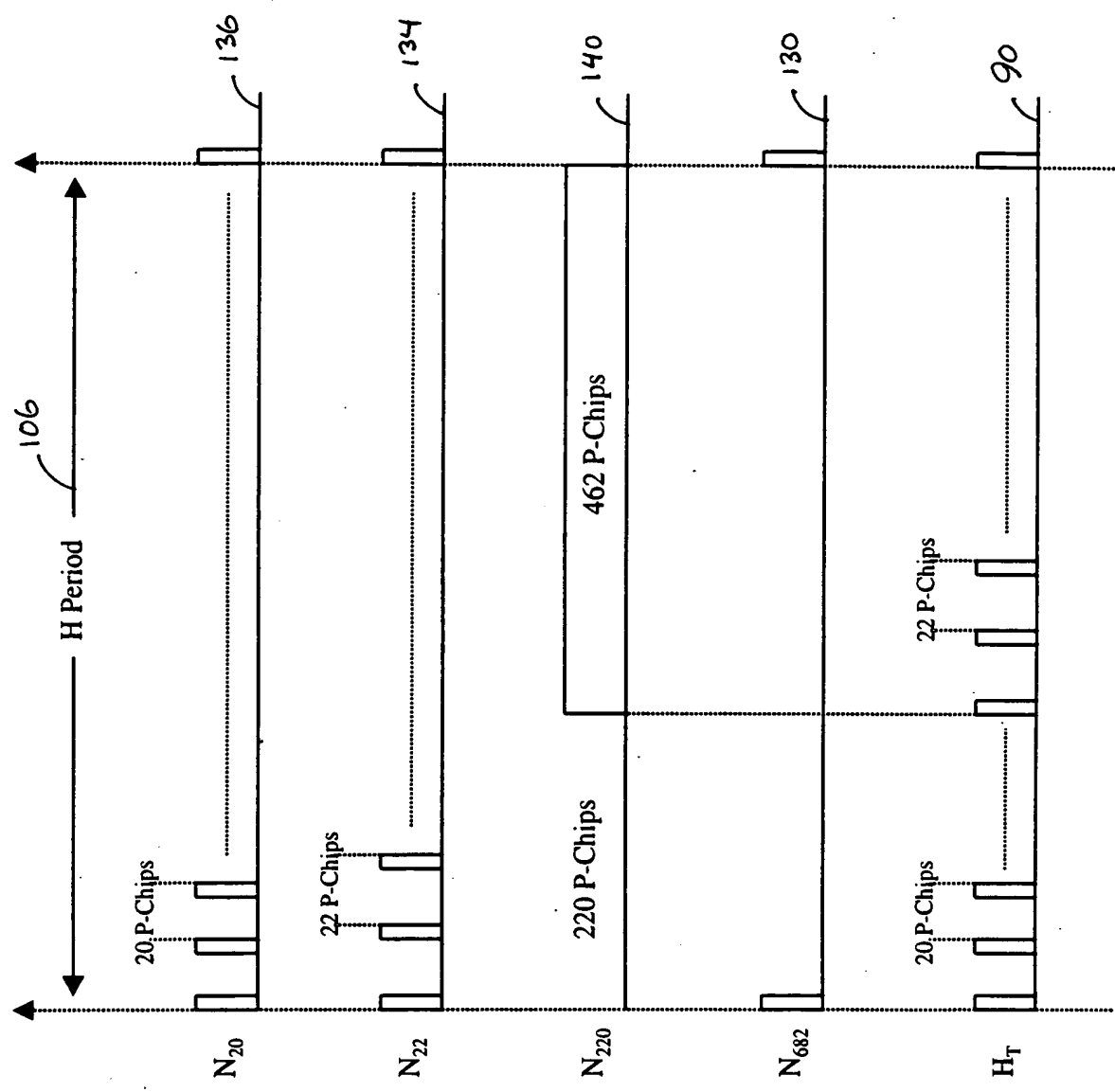


Figure 8 - H Period Generator Timing

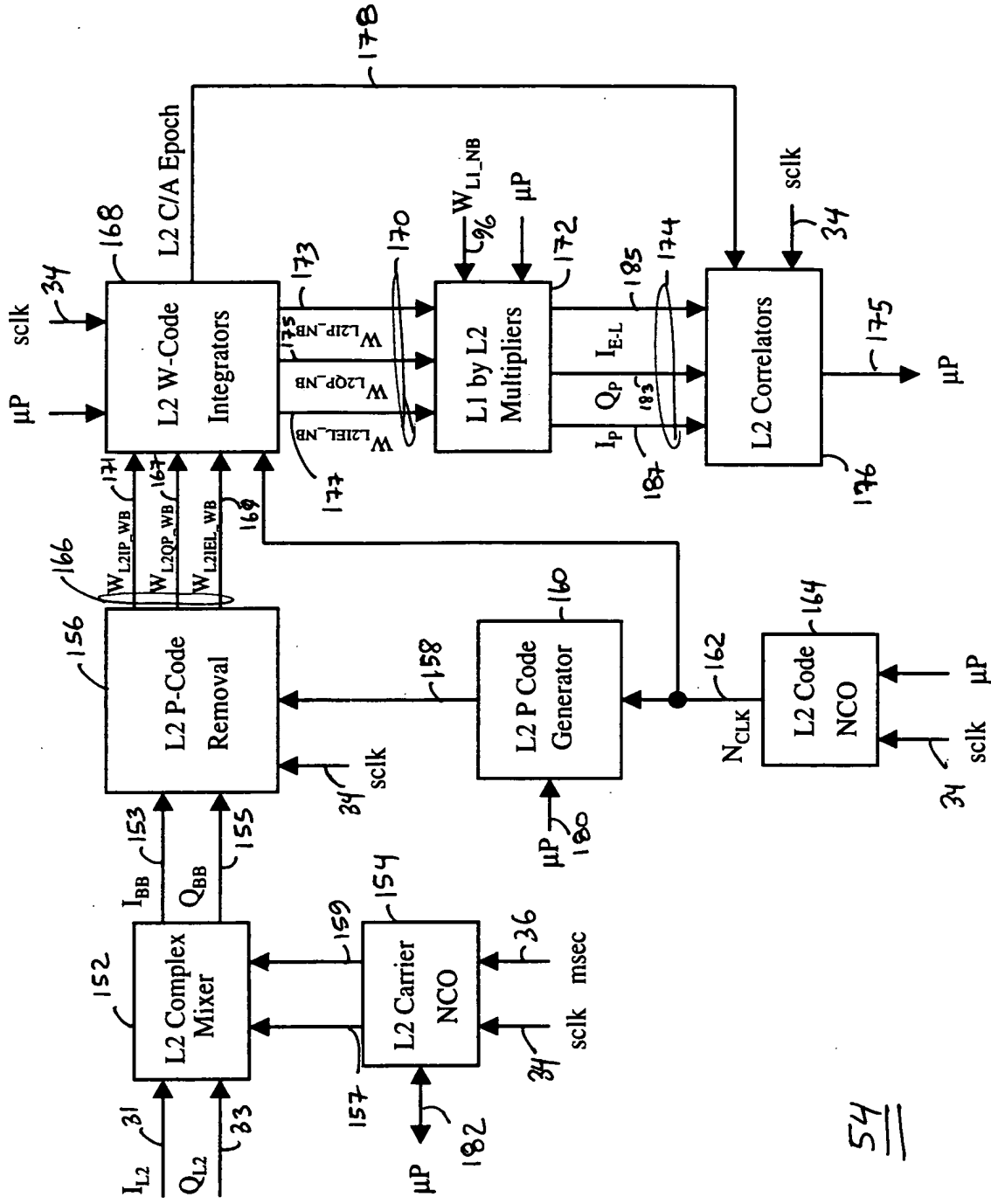


Figure 9 - L2 Tracker

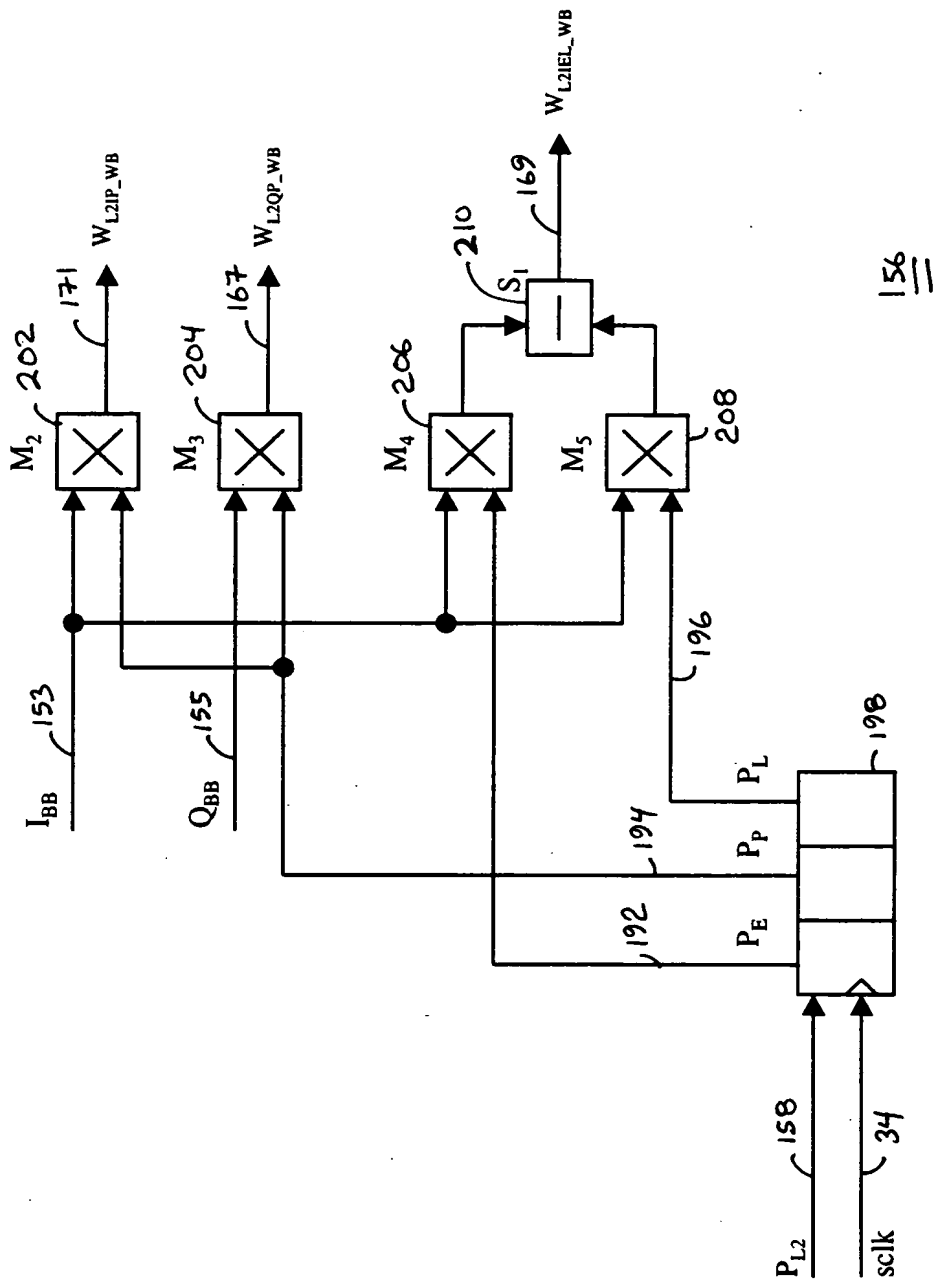


Figure 10 - L2 P-Code Removal

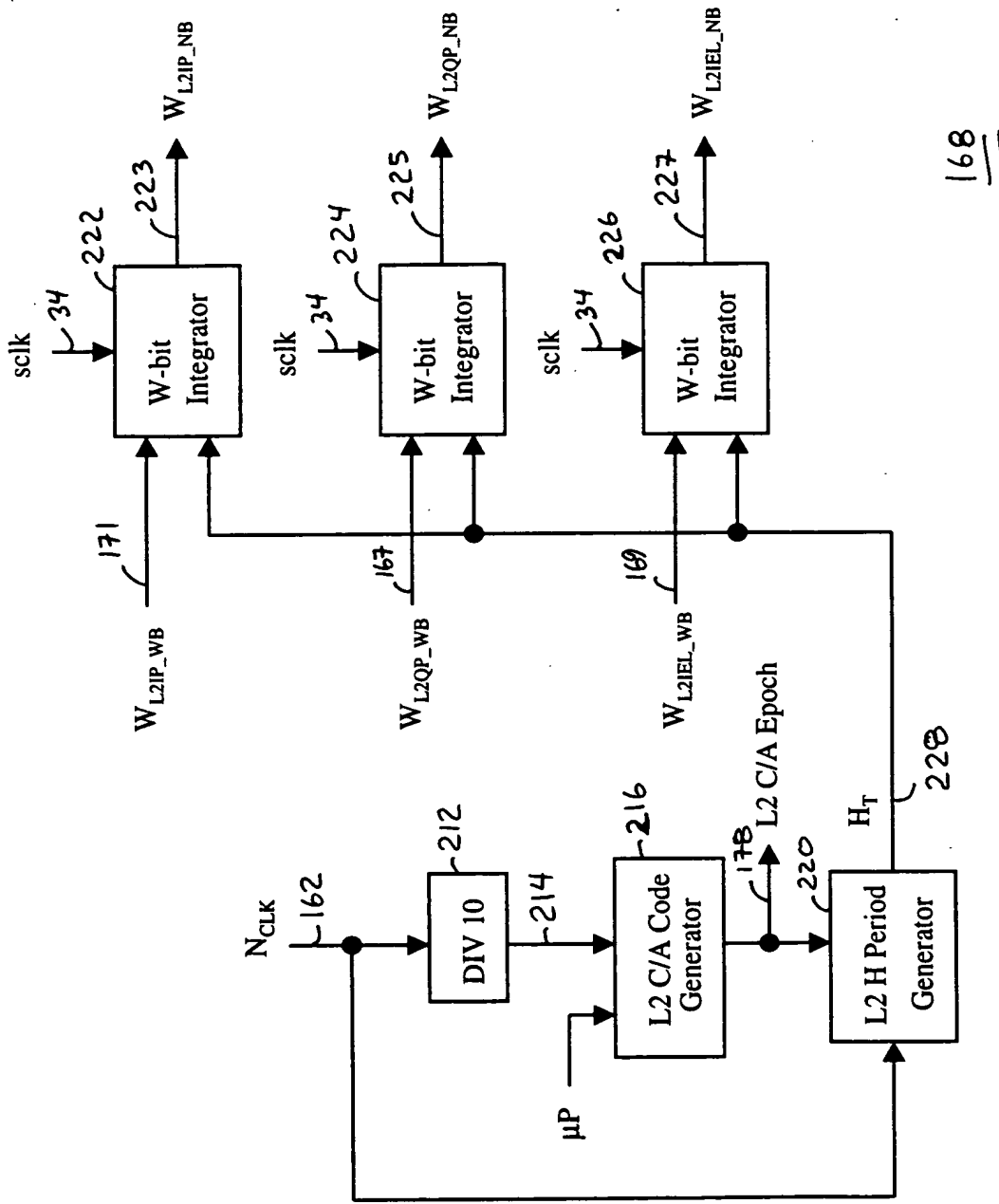


Figure 11 - L2 W-Code Integrators

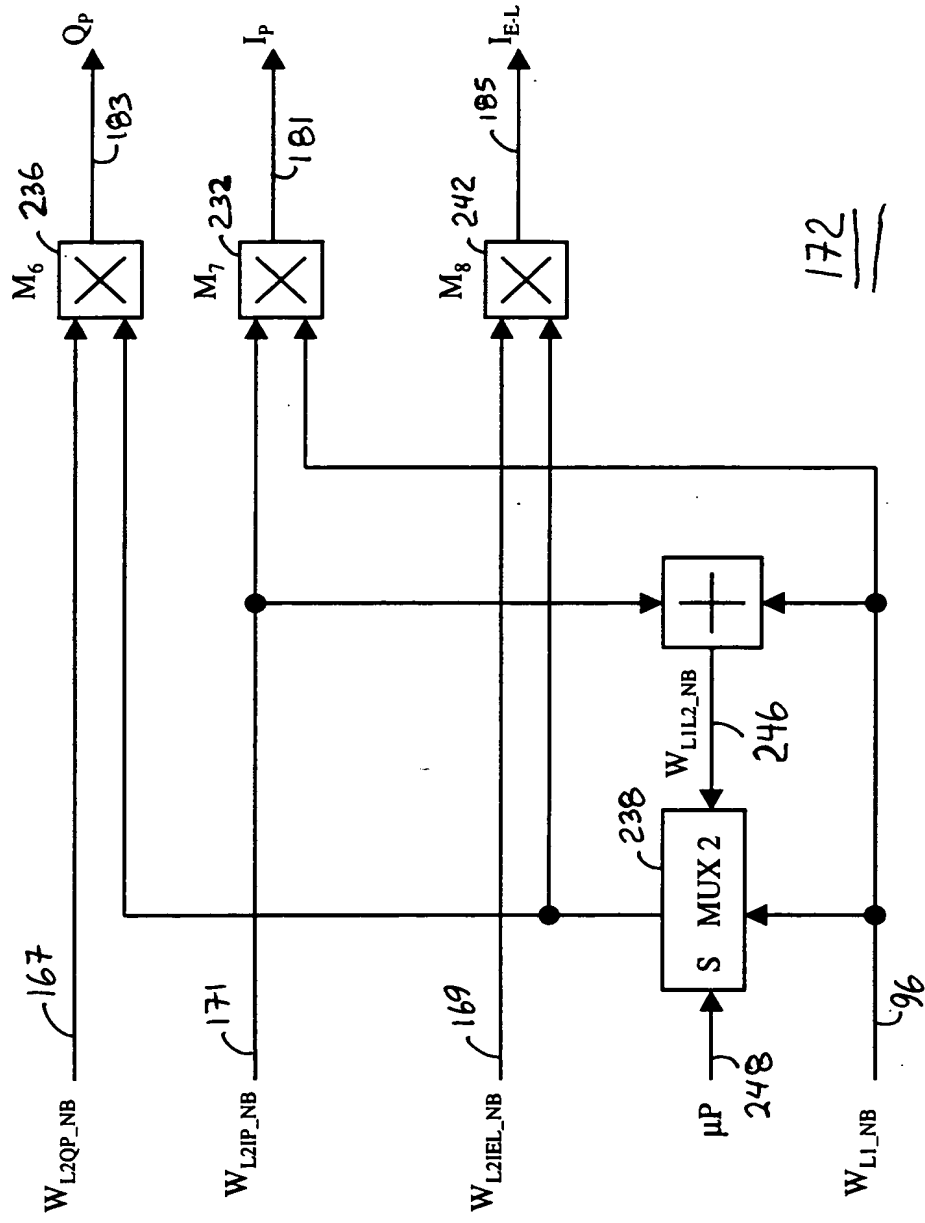
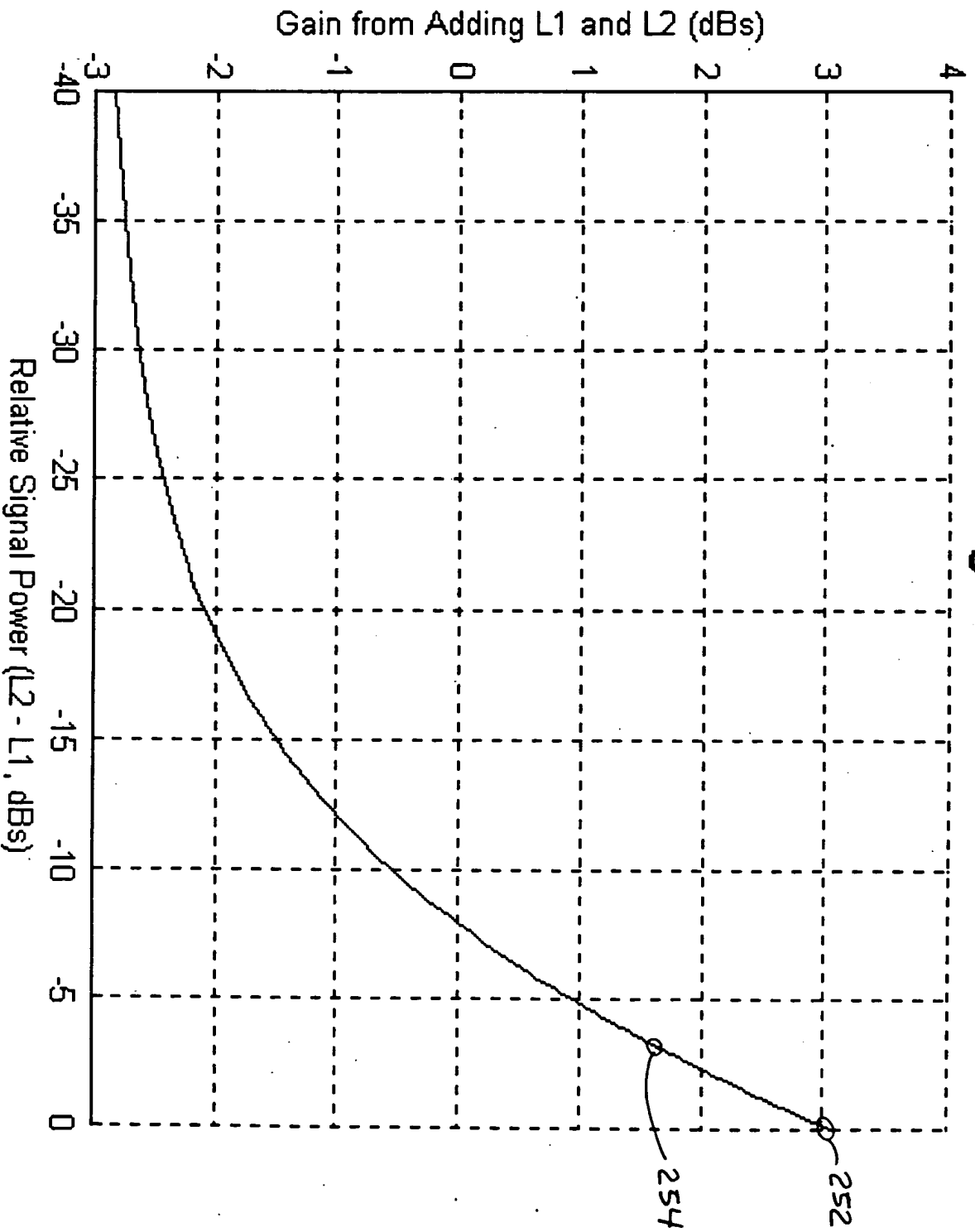


Figure 12 - L1 by L2 Multipliers

Figure 13



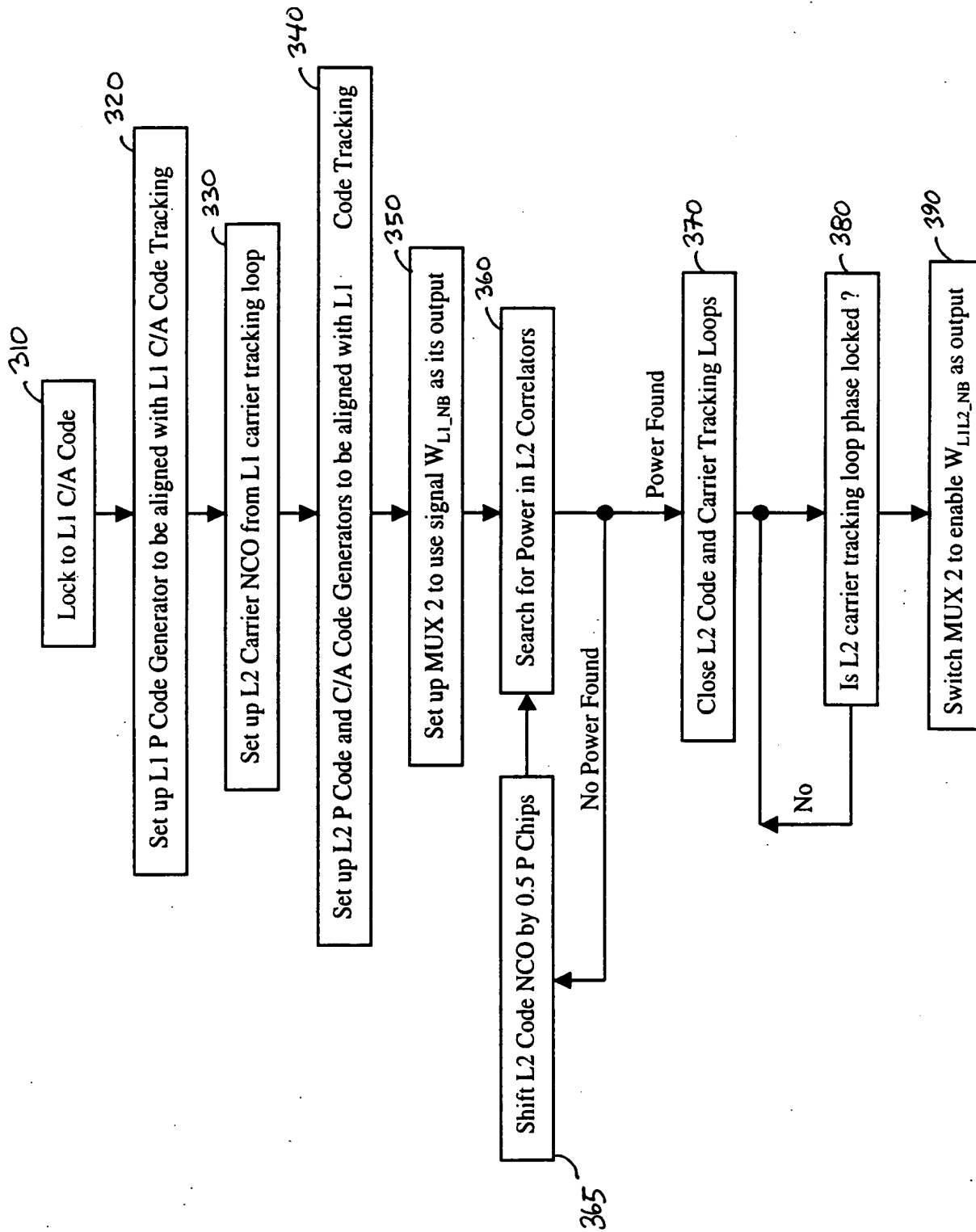
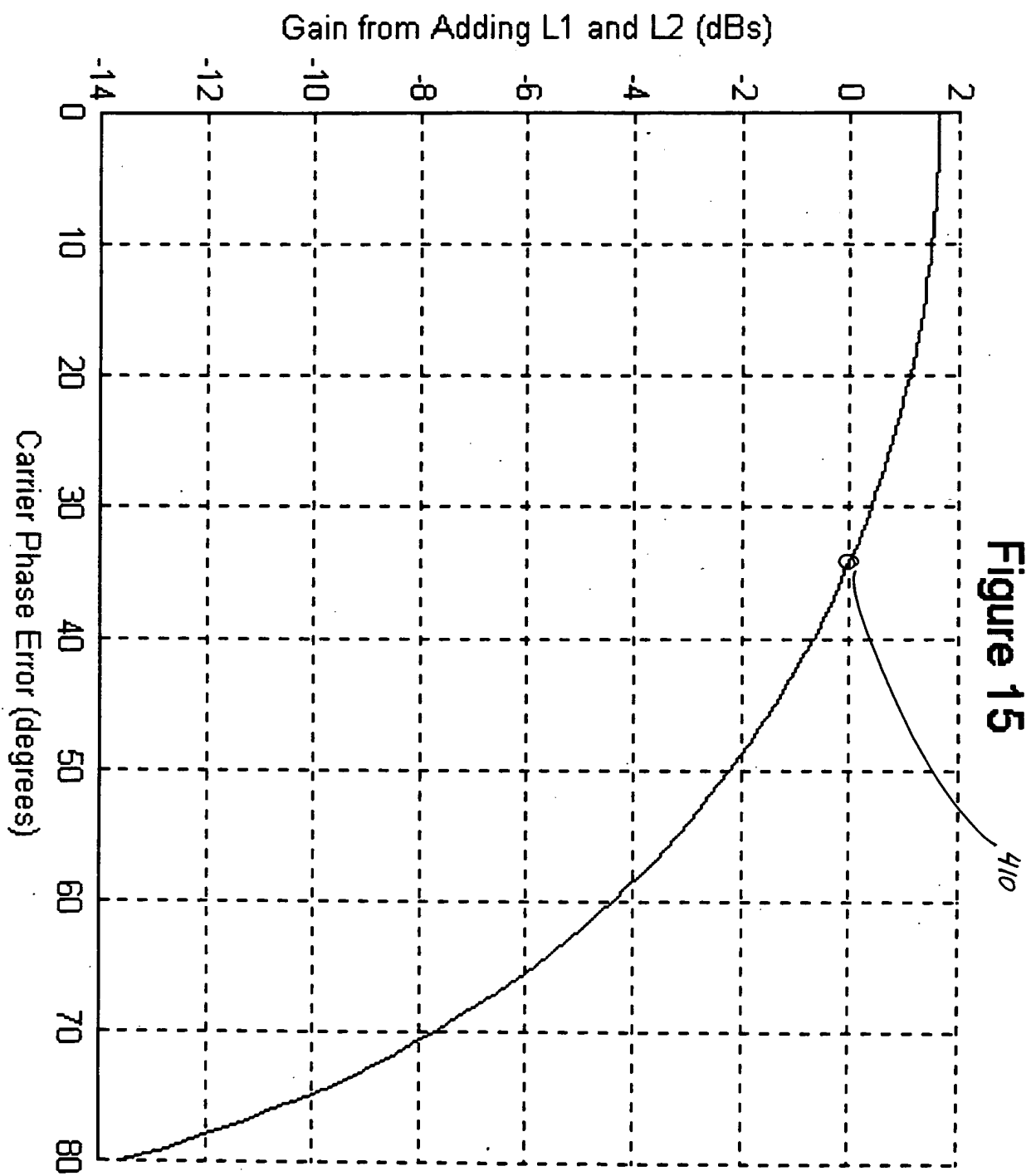


Figure 14 - Locking to L2 method



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